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APPLICATION NO.	F	ILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,813		03/29/2004	Shunichi Abe	403031	9714
23548	7590	12/20/2004		EXAMINER	
		MAYER, LTD	GRAYBILL, DAVID E		
SUITE 300	700 THIRTEENTH ST. NW SUITE 300			ART UNIT	PAPER NUMBER
WASHING	TON, DC	20005-3960	2822		

DATE MAILED: 12/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)				
	10/810,813	ABE ET AL.				
Office Action Summary	Examiner	Art Unit				
	David E Graybill	2822				
The MAILING DATE of this communication a Period for Reply	ppears on the cover sheet with the	correspondence address				
A SHORTENED STATUTORY PERIOD FOR REF THE MAILING DATE OF THIS COMMUNICATION  - Extensions of time may be available under the provisions of 37 CFR after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a rr - If NO period for reply is specified above, the maximum statutory perions  - Failure to reply within the set or extended period for reply will, by state Any reply received by the Office later than three months after the mail earned patent term adjustment. See 37 CFR 1.704(b).	N. 1.136(a). In no event, however, may a reply be ti eply within the statutory minimum of thirty (30) da od will apply and will expire SIX (6) MONTHS fron ute, cause the application to become ABANDONI	mely filed ys will be considered timely. n the mailing date of this communication. ED (35 U.S.C. § 133).				
Status	•					
1)⊠ Responsive to communication(s) filed on 26	August 2004.					
	nis action is non-final.					
	Since this application is in condition for allowance except for formal matters, prosecution as to the ments is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Disposition of Claims						
4) ☐ Claim(s) 8-12 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration.  5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 8-12 is/are rejected.  7) ☐ Claim(s) is/are objected to.  8) ☐ Claim(s) are subject to restriction and/or election requirement.						
Application Papers	,					
9) ☐ The specification is objected to by the Exami  10) ☑ The drawing(s) filed on 19 March 2004 is/are  Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct of the oath or declaration is objected to by the	e: a) accepted or b) objected on because one drawing(s) be held in abeyance. Seection is required if the drawing(s) is old	ee 37 CFR 1.85(a). ojected to. See 37 CFR 1.121(d).				
Priority under 35 U.S.C. § 119						
<ul> <li>12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).</li> <li>a) All b) Some * c) None of:</li> <li>1. Certified copies of the priority documents have been received.</li> <li>2. Certified copies of the priority documents have been received in Application No. 09/892,539.</li> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</li> <li>* See the attached detailed Office action for a list of the certified copies not received.</li> </ul>						
Attachment(s)  1) Notice of References Cited (PTO-892)  2) Notice of Draftsperson's Patent Drawing Review (PTO-948)	4)	Date				
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/0 Paper No(s)/Mail Date <u>4 pages</u> .		Patent Application (PTO-152)				

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In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 8-11 are rejected under 35 U.S.C. 102(a) as being clearly anticipated by Chun (6043430).

At column 2, line 66 to column 4, line 21, Chun discloses a semiconductor device TSOP (Thin Small Outline) Package having; upper (in second package 27') and lower (in first package 27) semiconductor chips 21 arranged between a first lead portion 23' and a second lead portion 23', respectively, on two opposing sides (the left and right sides in FIG. 7) of said semiconductor device, in plan view; a first die pad 23 integrated with and not coplanar with said first lead portion and located on one side of a an inherent reference plane passing through a central position between a first surface and a second surface of said first and second lead portions; and a second die pad 23 integrated with and not coplanar with said second lead portion and located on a second side of the reference plane, wherein said lower semiconductor chip is inherently supported by said first die pad and

said upper semiconductor chip is inherently supported by said second die pad portion, said upper and lower semiconductor chips are partially overlapping and overlap in height with said first and second lead portions; including: a first lead frame 23' connected to said first die pad and located, with said first lead portion, on the first side of said reference plane, and a second lead frame 23' connected to said first die pad and located, with said second lead portion, on the second side of said reference plane; wherein said first die pad portion is L-shaped and includes a first extension extending from an end of said first lead portion toward said second lead portion, and a first opposing portion continuing from said first extension and extending parallel to said first lead portion, said second die pad portion is arranged, in plan view, opposite said first die pad, is L-shaped, and includes a second extension extending from an end of said second lead portion toward said first lead portion and a second opposing portion continuing from said second extension and extending parallel to said second lead portion, said first extension and said first opposing portion have bottom surfaces inherently. supporting said lower semiconductor chip, and said second extension and said second opposing portion have upper surfaces inherently supporting said upper semiconductor chip; wherein said first and second lead portions and said first and second die pads are integrated (via the elements of the packages) into a common lead frame, said reference plane passes centrally

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(situated at or near the center) through the thickness of said lead frame, said first die pad supports said lower semiconductor chip of said partially overlapped upper and lower semiconductor chips, and said second die pad supports said upper semiconductor chip.

To further clarify the disclosure that the first and second die pads are not coplanar with the first and second lead portions, respectively, it is noted that even where they abut, the pads and portions do not lie in the same plane, but at most, lie only on the same plane.

To further clarify the disclosure that the chips are partially overlapping, in the partial view of FIG. 7 the chips are at least partially overlapping.

Also, to further clarify, Chun discloses first and second lead frames 23' because Chun discloses metal frames 23' which inherently provide support for the chips as well as electrical leads 23' to interconnect the integrated circuit on the chip, as the term lead frame is defined in the Manual of Classification, class 257 glossary.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

<sup>(</sup>a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chun (6043430).

Chun is applied as it is applied supra.

Also, Chun discloses adhesive layers 22' respectively bonding said upper and lower semiconductor chips to said first and second die pads wherein a center of the thickness of said first die pad portion and a center of the thickness of said second die pad portion are spaced from said reference plane in respective opposite directions,

However, Chun does not appear to explicitly disclose wherein the centers are spaced each by a distance equal to the sum of one-half the thickness of said lead frame and one-half the thickness of said adhesive

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layers bonding said upper and lower semiconductor chips to said first and second die pads.

Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose this particular distance because applicant has not disclosed that, in view of the applied prior art, the distance is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical, and it appears prima facie that the process would possess utility using another distance. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

For information on the status of this application applicant should check PAIR: Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

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have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is (703) 872-9306.

David E. Graybill Primary Examiner Art Unit 2827

D.G. 12-Dec-04